Investigation on Latch-Up Path between I/O PMOS and Core PMOS in a 0.18-µm CMOS Process

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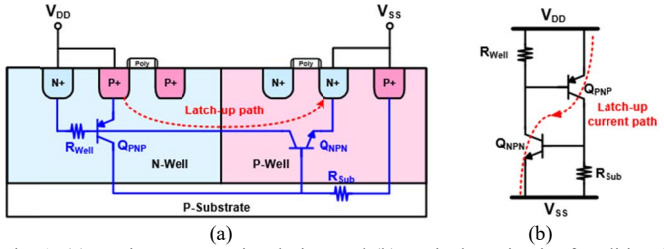
***Abstract*— This work studied the latch-up path between two PMOS devices powered by different supply voltages in a 0.18-µm CMOS process. In IC field applications, such a non-typical latch-up path between two PMOS devices was ever fired to cause unrecoverable failures. Through the silicon test chip, the latch-up path between I/O PMOS and core PMOS was investigated in details. The measurement results from the silicon chip with split test structures can be used to investigate the design rules on anode-to-cathode spacing and guard ring placement to prevent such PMOS-to-PMOS latch-up issue. In chip layout of IC products, the PMOS devices in different power domains shall be carefully checked to prevent the occurrence of such unexpected latch-up path.**

Index Terms-- latch-up, guard ring, design rule, holding voltage.

I. INTRODUCTION

The parasitic p-n-p-n structure between PMOS and NMOS historically caused latch-up events in CMOS integrated circuits (ICs). The parasitic silicon-controlled rectifier (SCR) structure in CMOS ICs between power lines of V_{DD} and V_{SS} may be accidentally triggered on to induce latch-up failures [1], [2]. The device cross-sectional view and the equivalent circuit of traditional latch-up path between V_{DD} and V_{SS} in a p-substrate bulk CMOS technology are shown in Fig. 1. When the vertical p-n-p BJT (Q_{PNP}) or the lateral n-p-n BJT (Q_{NPN}) is turned on, the latch-up mechanism of positive feedback regeneration will be initiated to generate a low-impedance path between the power lines [3]. The huge current generated from latch-up will pass through the p-n-p-n path to burn out the metal line and device structures. In accordance with the latch-up phenomenon, some solutions were reported to effectively prevent ICs from latch-up failure, such as process methods [4]-[7], layout placements [8], and circuit of active guard ring [9].

Joint Electron Device Engineering Council (JEDEC) had already defined the test standards with positive and negative current tests (I-tests) to examine the latch-up immunity. The specifications of the force current level under latch-up I-test in JESD78D is listed in Table I [10], where the largest trigger current level is up to 200 mA. Although the later standard JESD78E [11] modified the highest latch-up I-test level back to 100 mA, many companies still improve their IC products with I-test level of 200 mA against latch-up event for better reliability consideration.



(a) (b)

Fig. 1. (a) Device cross-sectional view and (b) equivalent circuit of traditional latch-up path between V_{DD} and V_{SS} in a p-substrate bulk CMOS technology.

TABLE I
TRIGGER SPECIFICATIONS IN LATCH-UP CURRENT TEST [10]

Latch-Up I-test	Range of Stress	Force Current
Positive I-Test	I	< 50 mA
	II	50 to < 100 mA
	III	100 to < 150 mA
	IV	150 to < 200 mA
	V	>= 200 mA
Negative I-Test	I	> -50 mA
	II	-50 mA to > -100 mA
	III	-100 to > -150 mA
	IV	-150 to > -200 mA
	V	< -200 mA

With the trend of system-on-chip (SoC) integration, more function and circuit blocks have been integrated into a single chip. To meet the application requirements and/or circuit specifications, some circuit blocks may be operated with different voltage levels. In the chip with multiple-voltage power supplies, the input/output (I/O) circuits powered by high supply voltage are typically integrated with the core circuits powered by low supply voltage to achieve high functionality and low power consumption. For example, as shown in Fig.2, the pre-buffer and output buffer are integrated in the same I/O cell with layout close to each other, where a latch-up path between two PMOS devices (M_{P2} and M_{P1}) powered by different voltages would be fired on. In such mixed-voltage applications, the non-typical latch-up event to cause unrecoverable failure was ever reported [12].

In this work, both anode-to-cathode spacings and guard ring parameters have been split to investigate the latch-up issue between two neighboring PMOS devices of different power domains in silicon chip with different test structures. In order to further examine the silicon data, the dc curve tracer (Tek370B) is used to verify the holding voltage (V_h) of each latch-up test structure, and more detailed examinations on latch-up immunity are verified by a commercial latch-up tester (Thermo Scientific MK.1) in the experimental measurement.

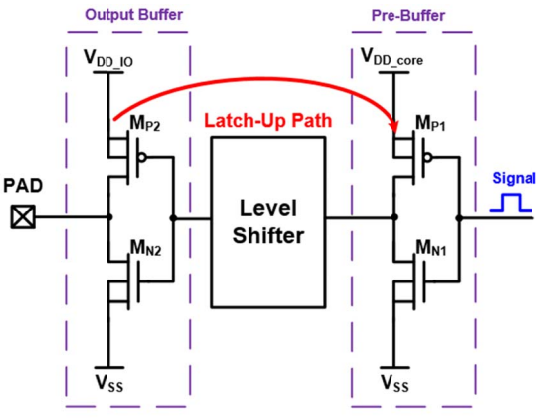


Fig. 2. The latch-up path between the pre-buffer and output buffer which are powered by different voltages and integrated in the same I/O cell.

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II. Test Structures

The latch-up test structures, composed of I/O PMOS (3.3V) and core PMOS (1.8V) in a 0.18-µm CMOS process, were studied in this work. The layout split parameters include anode-to-cathode spacings (Spacing), guard ring structures, and guard ring widths (GW). The cross-sectional views of the test structures with different guard ring surroundings are shown in Figs. 3(a) – 3(d) with the split names of type A, B, C, and D, respectively. Test structure A consists of a pair of an I/O PMOS and a core PMOS without inserting guard ring between them. The latch-up path is formed from the P+ diffusion (source of I/O PMOS, connected to $V_{DD\_I/O}$), the N-well of I/O PMOS, the p-well/p-substrate, to the N-well (connected to V_{DD_core}) of core PMOS. Test structure B comprises the device pair, and the I/O PMOS is surrounded by an N+ guard ring which is recognized as the base ring for I/O PMOS. Test structure C contains the device pair, and a row of P+ guard ring is placed between them and close to I/O PMOS. Test structure D combines the test structures of B and C together, where the I/O PMOS is surrounded by an N+ guard ring which a row of P+ guard ring is close to. In addition, the width of the P-Well in the latch-up path is mainly extended to investigate the latch-up risk of this test structure.

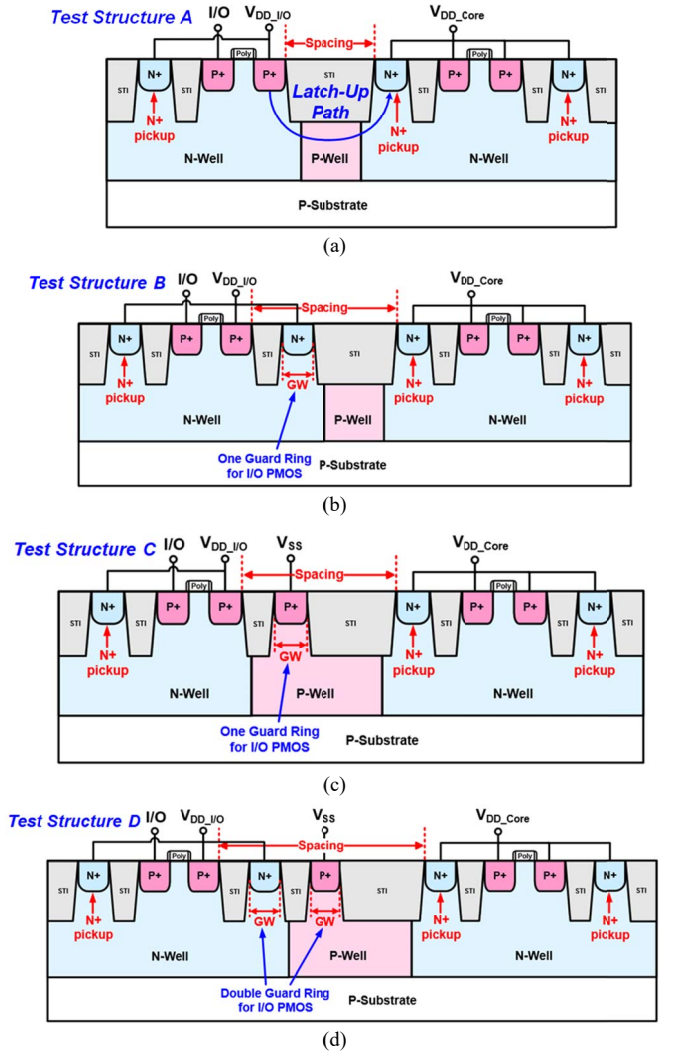

Fig. 3. The cross-sectional views of the latch-up test structures (a) A, (b) B, (c) C, and (d) D, where the latch-up path is formed between an I/O PMOS and a core PMOS.

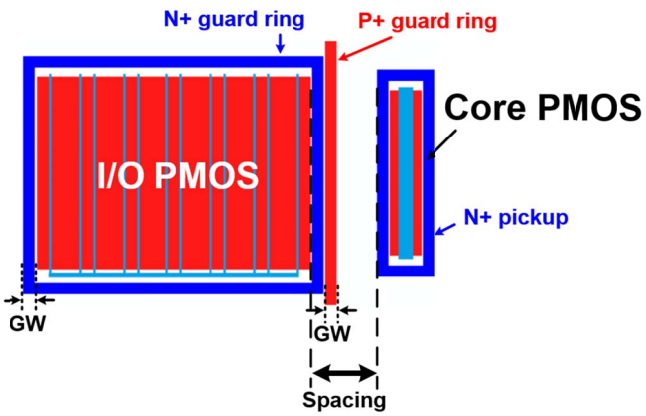

Fig. 4. Simplified layout top view of test structure D with the related layout parameters and placement.

Fig. 4 shows the layout top view of test structure D to illustrate the layout parameters. The device dimension of the I/O PMOS with a total channel width of 420 µm is larger than that of the core PMOS, which are drawn with a total width of 30 µm. These two PMOS devices are placed close to each other in layout with split spacings and/or guard rings for latch-up investigation.

III. Experimental Results

The testchip with such non-typical latch-up path between I/O PMOS and core PMOS was fabricated in a 0.18-µm 1.8/3.3-V CMOS technology, and the chip photograph of all test structures to investigate such non-typical latch-up paths are shown in Fig. 5.

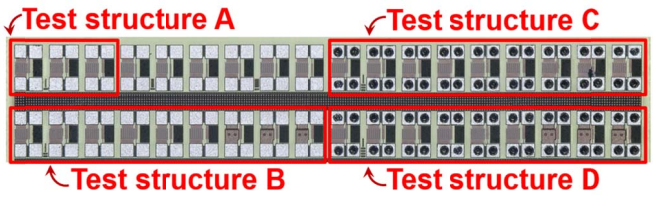

Fig. 5. Chip photograph of all test structures to investigate the latch-up issue between I/O PMOS and core PMOS powered with different power domians.

A. DC I-V Characteristics

Figure 6 shows the dc *I-V* characteristics of the test structures, measured by the curve tracer (Tek370B) at 25 °C, traced from $V_{DD\_I/O}$ to V_{DD_Core} with an anode-to-cathode spacing of 12 µm and a guard ring width of 2 µm. Based on the latch-up criterion, the latch-up risk cannot be ignored if V_h of the test structures is lower than the voltage differences between power domains. The latch-up path of test structures cross $V_{DD\_I/O}$ (3.3 V) and V_{DD_Core} (1.8 V). As a result, the latch-up may be fired once the V_h of test structures is below the voltage difference (ΔV = 1.5 V) between $V_{DD\_I/O}$ and V_{DD_Core}.

Further, to examine the latch-up risk, the measured relations between V_h and anode-to-cathode spacings under different guard ring widths for all test structures are shown in Fig. 7. In this figure, the V_h of the test structure A without any guard ring is lower than ΔV (1.5 V), obviously. For the test structure C with an anode-to-cathode spacing of above 8 µm and a guard ring width of above 0.42 µm, the latch-up occurrence can be avoided because the V_h is greater than ΔV (1.5 V).

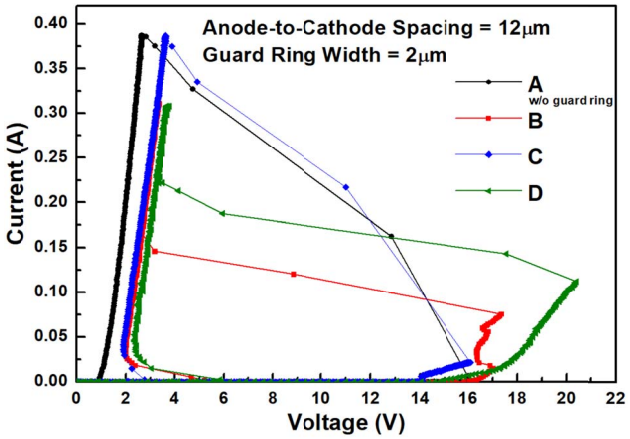

Fig. 6. The measured dc *I–V* characteristics of the test structures with an anode-to-cathode spacing of 12 μm and a guard ring width of 2 μm.

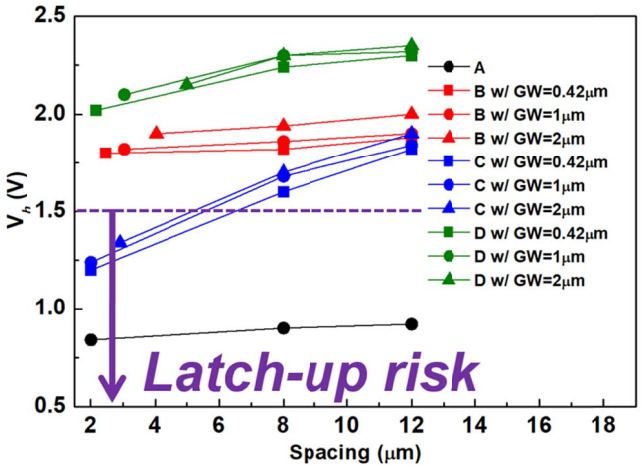

Fig. 7. Relations between V_h and anode-to-cathode spacings under different test structures and guard ring widths.

B. *Latch-Up Trigger Current Test*

Referring to [8], the n-type cathodes in a P-type substrate are most sensitive to positive current injection, and as a result this pulse polarity was used for the analysis. Figure 8 illustrates the measurement setup of JEDEC latch-up trigger current test. The device under test (DUT) is initially biased at normal circuit operating voltage of 3.3 V (V_{DD_IO}) and 1.8 V (V_{DD_Core}) with a positive current pulse applied to the I/O pin that connected to the drain of the I/O PMOS. The voltage and current waveforms on the DUT are monitored by the oscilloscope. When the trigger current pulse with a pulse width of 10 ms is injected to I/O pin, the latch-up event can be judged by monitoring the decrease on voltage waveform of the V_{DD_IO} pin.

In Figs. 9(a) and 9(b), the waveforms are the measured results of test structure A with an anode-to-cathode spacing of 12 μm under latch-up positive I-test of 2 mA, and 5 mA, applied to the I/O pin, respectively. In Fig. 9(a), after the I-test of 2 mA, the voltage level of V_{DD_IO} is still kept at 3.3 V. This implies that no latch-up event happened under such a trigger current injection. However, in Fig. 9(b), the voltage level of V_{DD_IO} is decreased to ~2.8 V after the I-test of 5 mA. The latch-up path between the I/O PMOS and the core PMOS was fired on by the trigger current injection of 5 mA. Therefore, the test structure A with an anode-to-cathode spacing of 12 μm can pass the I-test of 2 mA, but fail under I-test injection of 5 mA.

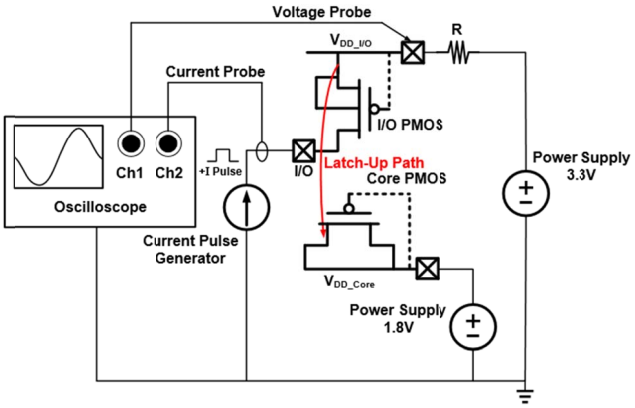

Fig. 8. Latch-up measurement on the test structure with the positive current pulse applied to the I/O pad (connected to the drain of I/O PMOS).

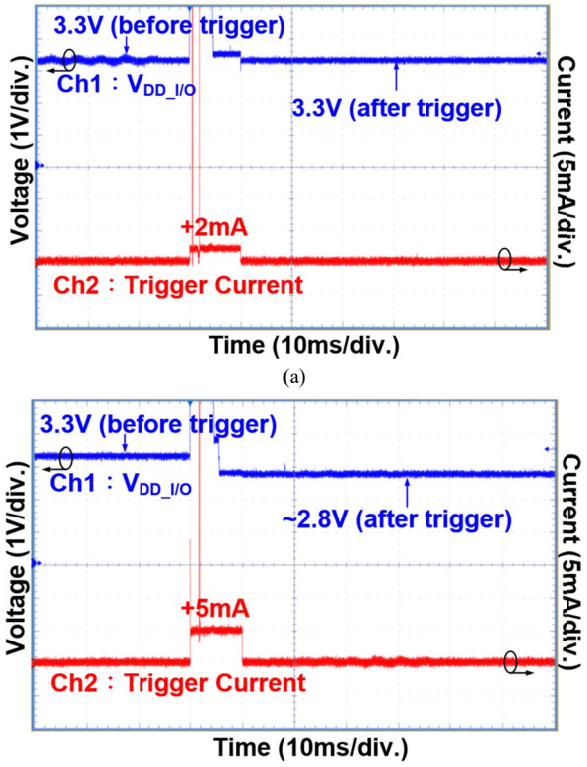

Fig. 9. Measured waveforms of test structure A with an anode-to-cathode spacing of 12 μm under latch-up positive I-test of (a) 2 mA, and (b) 5 mA, applied to the I/O pin that connected to the drain of I/O PMOS.

Moreover, to enhance the accuracy of measured data and detailed examination, a commercial latch-up test machine (Thermo Scientific MK.1) with a pulse width of 10 ms, a slew rate of 100V/1ms, and a pulse step of 1 mA have been commonly used in IC industry to verify the latch-up immunity. In the standard JESD78D, the highest immunity level was ever set at 200 mA, therefore some companies adopted this level as their latch-up specification of IC products. The relations between V_h, anode-to-cathode spacings, and latch-up immunities are shown in Fig. 10, where the latch-up I-test immunity results were measured at 125°C of environment temperature. The hollow marker expresses the latch-up immunity of the test structure is below 200 mA. In this way, it is realized that the test structures, whose V_h are lower than 1.5 V, really have suffered latch-up failures.

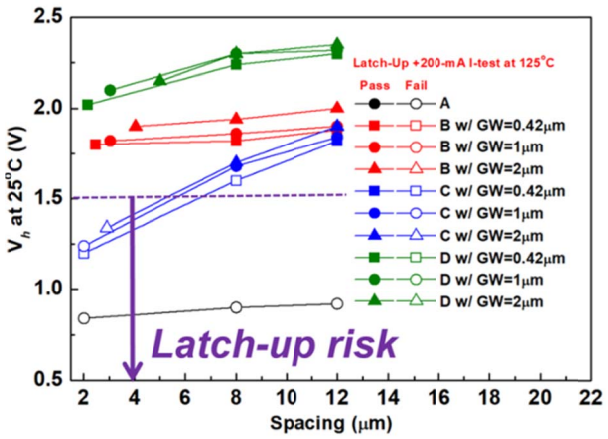

Fig. 10. Relations between V_h, anode-to-cathode spacings, and latch-up I-test immunity, where $V_{DD\_I/O}$ is biased at 3.3 V and V_{DD_Core} is biased at 1.8 V, for all test structures under different types and guard ring widths.

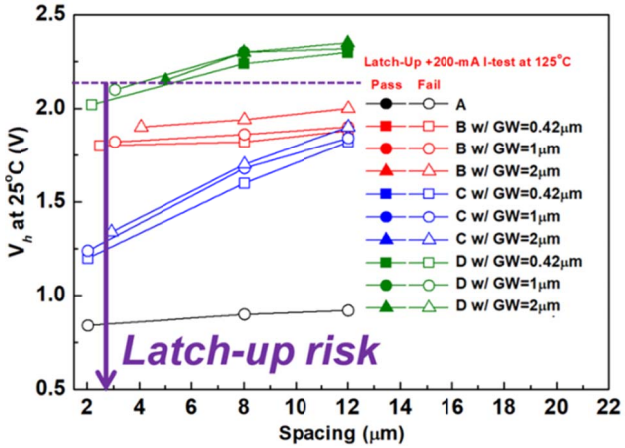

Fig. 11. Relations between V_h, anode-to-cathode spacings, and latch-up I-test immunity, where $V_{DD\_I/O}$ is biased at 3.63 V and V_{DD_Core} is biased at 1.5 V, for all test structures under different types and guard ring widths.

However, the supply voltages of $V_{DD\_I/O}$ and V_{DD_Core} may have some variation during circuit operations. With the irregular condition, $V_{DD\_I/O}$ may be biased at 3.63 V (1.1 times V_{DD}), but V_{DD_Core} may be biased at 1.5 V only. Therefore, the voltage difference (ΔV) between $V_{DD\_I/O}$ and V_{DD_Core} becomes 2.13 V. For the test structures, the relations between V_h, anode-to-cathode spacings, and latch-up I-test immunities are shown in Fig. 11, with $V_{DD\_I/O}$ of 3.63 V and V_{DD_Core} of 1.5 V. The latch-up path can be successfully blocked in the test structure D with an anode-to-cathode spacing of above 8 μm and a guard ring width of above 1 μm.

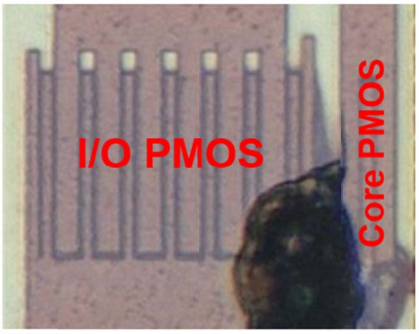

Fig. 12. OM photograph to identify the latch-up failure located on the test structure C with a 0.42-μm guard ring width and an 8-μm anode-to-cathode spacing after latch-up positive I-test.

To further identify the latch-up failure locations, the optical microscope (OM) inspection was used. After latch-up current test, the latch-up induced damage on the test structure C is found and shown in Fig. 12. The latch-up current flowing through the silicon chip caused serious irrecoverable burned-out failure, which obviously located at the path between I/O PMOS and core PMOS.

IV. Conclusions

The latch-up issue between I/O PMOS and core PMOS has been investigated. The measured results in silicon chip have proved that the p-n-p-n path between two neighboring PMOS devices powered by different voltages is really sensitive to latch-up event. In the design rules, the corresponding latch-up prevention on this situation was not mentioned or specified in detail. As a result, the foundry in semiconductor industry must split more testkeys with different layout parameters to formulate the corresponding design rule against the non-typical latch-up path presented in this work. The IC design houses shall check their chip layout by EDA tools to verify whether their chip has high latch-up risk among the neighboring PMOS devices powered with different voltage levels.

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